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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,872	02/26/2002	Joseph A. Iadanza	BUR920010100	6213

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SCHMEISER, OLSEN + WATTS
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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,872	IADANZA, JOSEPH A.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *23-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-16 are rejected under 35 U.S.C. § 102 (e) as being anticipated by Bohr (U.S. Patent No. 6,617,681). With regard to Claim 1, Bohr teaches a predefined block of functional circuitry (140) having a plurality of I/O pins (118) and a backside I/O pad electrically connected to each I/O pin through a backside via (122) of an integrated circuit. See figures 4 and 6.

With regard to Claim 2, Bohr teaches I/O pins (118) formed in a lower interconnect level of an integrated circuit chip. See figures 4 and 6.

With regard to Claim 3, Bohr teaches I/O pins (118) formed in a lowest interconnect level of an integrated circuit chip. See figures 4 and 6.

With regard to Claim 4, Bohr teaches an integrated circuit that is fabricated using a bulk silicon substrate (116). See column 5, lines 65-66.

With regard to Claim 5, Bohr teaches predefined circuitry (140) that includes a first portion containing functional circuitry (142, 144) and a second portion containing I/O pins (118). See figures 4 and 6.

With regard to Claim 6, Bohr teaches a backside via (122) that connect to the I/O pins (118) in the second portion. See figures 4 and 6.

With regard to Claim 7, Bohr teaches a plurality of frontside I/O pads for the I/O pins (118) and additional I/O pins (see figure 6), each additional I/O pin electrically connected to one frontside pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 8, Bohr teaches a structure that includes non-predefined circuitry (see column 6, lines 63-67 and column 7, lines 1-9).

With regard to Claim 9, Bohr teaches a plurality of frontside I/O pads for the I/O pins (1 18) and the non-predefined circuitry having a plurality of I/O pins (see column 6, lines 63-67 and column 7, lines 1-9), each additional I/O pin of the non-predefined circuitry electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 10, Bohr teaches additional predefined circuit I/O pins (see column 6, lines 63-67 and column 7, lines 1-9), each additional predefined circuit I/O pin of the non-predefined

circuitry electrically connected to one frontside I/O pad of the integrated circuit by a global wiling connection.

With regard to Claim 11, Bohr teaches providing a predefined block of functional circuitry (140) having a plurality of I/O pins (118) and connecting a backside I/O pad electrically connected to each I/O pin through a backside via (122) of an integrated circuit. See figures 4 and 6.

With regard to Claim 12, Bohr teaches providing additional I/O pins and electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 13, Bohr teaches providing non-predefined circuitry (see column 6, lines 63-67 and column 7, lines 1-9).

With regard to Claim 14, Bohr teaches providing a plurality of frontside I/O pads for the I/O pins (118) and electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 15, Bohr teaches providing additional predefined circuit I/O pins (see column 6, lines 63-67 and column 7, lines 1-9), and electrically connecting each additional I/O pin to one I/O frontside pad of the integrated circuit by a global wiring connection.

With regard to Claim 16, Bohr teaches forming a backside via (122) in a bulk silicon substrate (116). See column 5, lines 65-66 and see figures 4 and 6.

Allowable Subject Matter

2. Claims 23-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

3. Applicant's arguments have been fully considered, but are not deemed persuasive for the reasons stated in the body of the office action. Applicant argues that, "*Applicants respectfully contend that Bohr does not anticipate claim, because FIGS. 4 and 6 of Bohr do not disclose "a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit*" and that "*Bohr do not depict an integrated circuit, but instead depict an interposer that couples an integrated circuit to a circuit board*'.

However, the examiner disagrees with Applicant's assertion of the Bohr reference. Although Bohr discloses an interposer (column 6, lines 16-62), it should noted that Bohr also discloses that "*By integrating various active and passive circuit elements in the interposer, it is possible to include circuit functionality into the interposer*" (column 6, lines 63-65), including *I/O buffer circuits* (column 7, lines 4-7). Therefore, as stated in the rejection, Bohr discloses a predefined

block of functional circuitry having a plurality of I/O pins and a backside I/O pad electrically connected to each I/O pin through a backside via of an integrated circuit, as claimed.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALLAN R. WILSON
PRIMARY EXAMINER

E.O.
A.U. 2815
7/11/04